

Thin n-in-p planar pixel modules for the ATLAS upgrade at HL-LHC

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Abstract

The ATLAS experiment will undergo a major upgrade of the tracker system in view of the high luminosity phase of the LHC (HL-LHC) foreseen to start around 2025. Thin planar pixel modules are promising candidates to instrument the new pixel system, thanks to the reduced contribution to the material budget and their high charge collection efficiency after irradiation. New designs of the pixel cells, with an optimized biasing structure, have been implemented in n-in-p planar pixel productions with sensor thicknesses of 270 μm . Using beam tests, the gain in hit efficiency is investigated as a function of the received irradiation fluence. The outlook for future thin planar pixel sensor productions will be discussed, with a focus on thin sensors with a thickness of 100 and 150 μm and a novel design with the optimized biasing structure and small pixel cells (50x50 and 25x100 μm^2). These dimensions are foreseen for the new ATLAS read-out chip in 65 nm CMOS technology and the fine segmentation will represent a challenge for the tracking in the forward region of the pixel system at HL-LHC. To predict the performance of 50x50 μm^2 pixels at high η , FE-I4 compatible planar pixel sensors have been studied before and after irradiation in beam tests at high incidence angle with respect to the short pixel direction. Results on cluster shapes, charge collection- and hit efficiency will be shown.

Keywords: Pixel detectors, Planar sensors, ATLAS, HL-LHC

1. Introduction

One of the main challenges for the innermost tracking detectors after the upgrade to the HL-LHC with an instantaneous luminosity of up to $5 \times 10^{-34} \text{ cm}^{-2} \text{ s}^{-1}$ will be the exposure to high radiation. The ATLAS pixel system will be prospectively exposed to particle fluences up to $2 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ (1 MeV neutron equivalent) [1, 2]. To maximize the hit efficiency and reduce the leakage current and power dissipation after irradiation, thin sensors are being developed. Sensors with a thickness of 100 and 150 μm were found to reach the same hit efficiency as thicker sensors already at a bias voltage of 300 V shown in Fig 1.

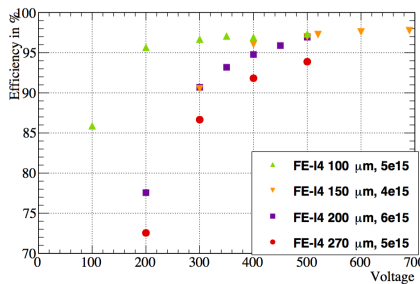


Figure 1: Comparison of hit efficiencies of FE-I4 modules with sensor thicknesses between 100 and 270 μm at an irradiation fluence of around $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$.

A highest hit efficiency of around 97% was obtained for perpendicular incident tracks at a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$, the

expected fluence for the second layer at HL-LHC [3]. The main inefficiencies are caused by the bias dot and the bias rail, as described in [4] for fluences up to $3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. In this paper, different designs of n-in-p planar hybrid pixel modules are investigated at the expected fluence of the second layer. Alternative biasing structures were implemented in a CiS sensor production with 270 μm thickness and compared to the standard design. To cope with the highest occupancy at HL-LHC, smaller pixel dimensions with respect to the ones presently implemented in the FE-I3 chip (50x400 μm^2) and the FE-I4 chip (50x250 μm^2), developed for the ATLAS Insertable B-Layer (IBL), are mandatory [5]. The new read-out chip for the ATLAS pixel systems at HL-LHC is being developed by the CERN RD53 Collaboration with a pixel cell of 50x50 μm^2 in the 65 nm CMOS technology and is expected to be ready at the beginning of 2017 [6, 7]. Sensors compatible with this chip have been implemented in a recent MPG-HLL pixel production with a thickness of 100 and 150 μm . First results on the electrical characterization of these devices will be shown.

2. Optimization of the pixel cell design

2.1. Test beam analysis of different pixel cell designs

In the present design of the ATLAS pixel sensors it is possible to bias the pixel via the punch-through mechanism with an n^+ implant dot implemented in the pixel cell, connected to the bias ring through an aluminium rail. It has been observed that these structures introduce a loss of efficiency after irradiation [3, 4]. To reduce this effect, an optimization has been carried out, comparing the performance of the different designs

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shown in Fig. 2. These were implemented in two FE-I4 compatible sensors in a CiS n-in-p production on 6" wafers with a thickness of 270 μm . The sensors were irradiated to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ and then studied with a beam test at CERN SPS. The hit efficiency was determined performing track reconstruction with EUTelescope software [9]. The systematic uncertainty associated to the efficiency measurements is 0.3%, as estimated in [10]. Also at this higher fluence the relative performance remained similar to the one observed at $3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$: the bias rail superimposed to the pixel implant as in Fig. 2b yields a higher hit efficiency with respect to the standard geometry. A still better hit efficiency was found for the common punch-through dot, placed externally to the pixel implant and serving four neighbouring pixels, Fig. 2c. This geometry was implemented in a $25 \times 500 \mu\text{m}^2$ pixel cell, still compatible with the FE-I4 chip.

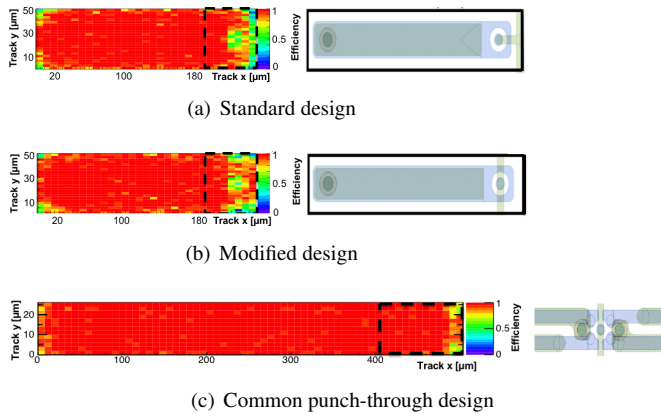


Figure 2: Hit efficiency for (a) the standard punch-through design and (b) the modified individual biasing structure where the bias rail is running over the bias dot after an irradiation fluence of $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. In addition the hit efficiency map of a pixel cell with the common punch-through design with modified dimensions to $25 \times 500 \mu\text{m}^2$ is illustrated in (c). Cut-offs of a $50 \times 50 \mu\text{m}^2$ pixel cell inside the $50 \times 250 \mu\text{m}^2$ pixel cell (a and b) and a $25 \times 100 \mu\text{m}^2$ pixel cell inside the $25 \times 500 \mu\text{m}^2$ pixel cell (c) are outlined. The modules were operated at 500 V.

At a bias voltage of 500 V a hit efficiency of 93.9% was obtained for the standard design where the new arrangement of the bias rail in the modified design in Fig. 2b improved the hit efficiency to 94.6%. The common punch-through yields even 96.0%, while it increases to 98.0% at 800 V. These values are about 3% lower than what was obtained at a fluence of $3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. The smaller pixel dimensions of the future pixel read-out chips are indicated in the pixel cells in Fig. 2 using a $50 \times 50 \mu\text{m}^2$ (a and b) and $25 \times 100 \mu\text{m}^2$ (c) pixel cell. A smaller pixel with the current designs would show even lower efficiencies. Therefore, further optimization of the biasing structures is mandatory. It is planned to repeat the hit efficiency measurements with sensors in a fluence range up to $10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ to confirm the better performance observed within the new biasing design.

2.2. Estimation of hit efficiency for a $25 \times 100 \mu\text{m}^2$ pixel cell

Since modules with small pixel cells are not available yet, the hit efficiency for a $25 \times 100 \mu\text{m}^2$ pixel cell at an irradiation fluence of $3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ was estimated based on the existing prototype of the $25 \times 500 \mu\text{m}^2$ pixel cell with the new common punch-through design. Since inefficiencies appear at the edges of the pixel caused by charge sharing as well as by the punch-through structure, the hit efficiencies in the first 40 μm and in the last 60 μm were combined to estimate the efficiency for an effective pixel cell of $25 \times 100 \mu\text{m}^2$. A value of 95.5% was obtained and is indeed lower compared to the $25 \times 500 \mu\text{m}^2$ pixel cell, but only a bit lower compared to the hit efficiency of 96.5% obtained with the standard implementation of the punch-through in a $50 \times 250 \mu\text{m}^2$ pixel cell.

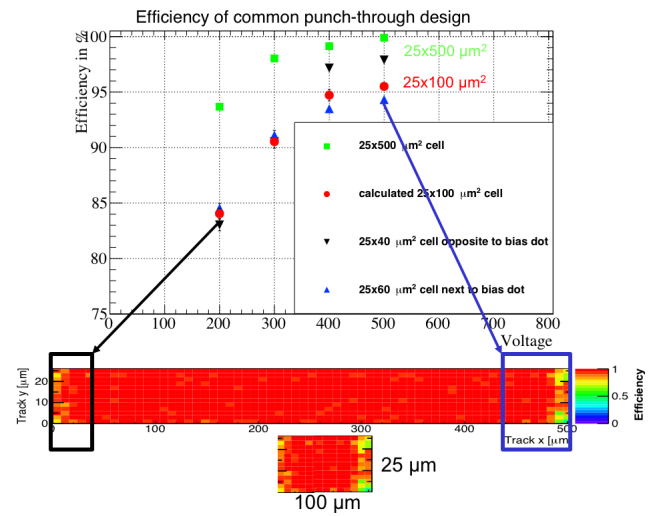


Figure 3: Estimated hit efficiency of a $25 \times 100 \mu\text{m}^2$ pixel cell irradiated at $3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ and compared to the hit efficiency of the larger $25 \times 500 \mu\text{m}^2$ pixel cell. Efficiencies at the edge regions are also shown separately.

3. Performance at high incident angle

Since smaller pixel cells are challenging for the tracking in high pseudo-rapidity regions (high η), the hit efficiency for a cell of $50 \times 50 \mu\text{m}^2$ at $\eta=2.5$ was determined. FE-I4 modules were placed in the beam at DESY and CERN SPS in such a way that the particles were crossing the pixel along the short side (50 μm) at an angle of $\theta=80^\circ$. Such measurements were previously performed at CERN with a 100 μm thick not irradiated module from the VTT production and at DESY with a 200 μm thick irradiated module from a CiS production. The cluster size along η strongly depends on the sensor thickness: thinner sensors produce smaller clusters and result in a lower pixel occupancy, as shown in Fig. 4. There was no possibility to reconstruct tracks for these data sets, implying that the analysis needs to be performed using the hit information of the long clusters compatible with the hypothesis a single particle passing through the sensor. Given the particle path of approximately 50

μm in each pixel cell, a collected charge of 3100 e was estimated [11]. Therefore, a dedicated tuning was performed with a low target threshold of 1000 e. A not irradiated 200 μm thick sensor was recently investigated in a beam test at CERN SPS again at $\theta=80^\circ$. An average cluster size of 20 pixels was reconstructed, slightly less than the expected value of 23-24. This was due to a misplacement of 2° of the module with respect to the nominal position.

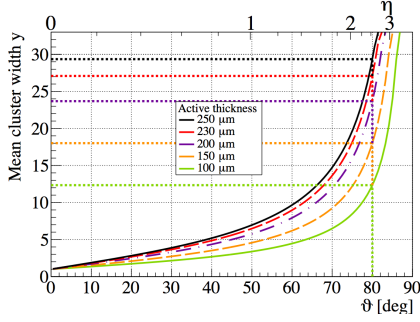


Figure 4: Mean cluster width along the short pixel cell side for an FE-I4 module placed at high θ in the beam, as a function of beam incidence angle. The relationship is also valid for a pixel sensor with a $50 \times 50 \mu\text{m}^2$ cell at high η with respect to the beam [3].

The collected charge is shown in Fig. 5 for the different pixels belonging to the cluster. It is almost constant over the sensor depth, except for the entrance and exit pixels that are not entirely crossed by the track. The obtained hit efficiency of a single pixel for the 200 μm thick sensor is 94.9% and hence it is (4-5)% lower than the one of 100 μm thickness presented in [4]. The hit efficiency was calculated with varying assumptions on the allowed number of holes between two pixels inside the cluster, up to a maximum of 10. The single hit inefficiency is the total number of holes divided by the cluster length not including the entrance and exit pixels that are 100% efficient by construction.

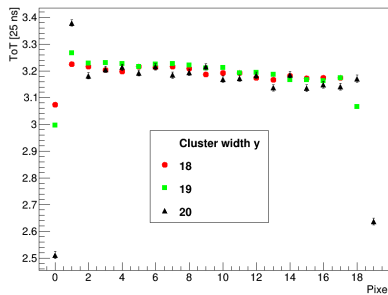


Figure 5: Charge collection expressed in units of Time over Threshold, as a function of pixel number for cluster size 18, 19 and 20 obtained with a not irradiated FE-I4 module employing a 200 μm thick sensor and tilted by 80° . The pixel number equal to zero correspond to the sensor back-side and 20 to the sensor front-side.

4. Novel pixel cell design

New pixel cells were designed, compatible with the $50 \times 50 \mu\text{m}^2$ grid of the read-out chip being developed by the RD53 Collaboration: one with the same cell size and an alternative version with $25 \times 100 \mu\text{m}^2$. For both designs the best performing biasing structures were combined. The common punch-through design was chosen together with the bias rail running as much as possible superimposed to the pixel implant. Both new layouts, displayed in Fig. 6, have been implemented in the recent MPG-HLL production described in the next section.

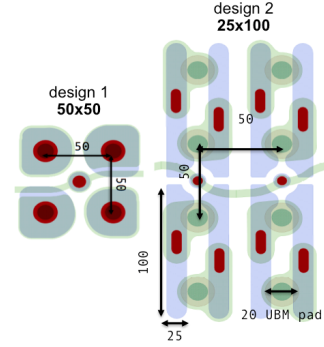


Figure 6: Novel pixel design of 50×50 and $25 \times 100 \mu\text{m}^2$ pixel cells combining the novel common punch-through design with the new arrangement of the bias rail being superimposed to the pixel implant as much as possible.

4.1. Sensor productions at CiS and MPG-HLL

At CiS, an innovative method was explored to produce thin sensors without the use of a handle wafer. The technology employs anisotropic KOH etching to create backside cavities in the wafer leaving thicker frames around each single structure.

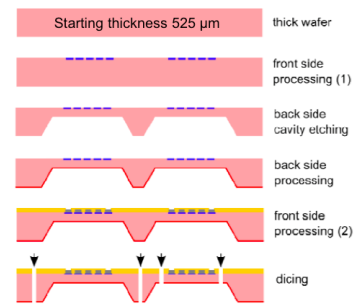


Figure 7: Production process flow at CiS technology [12].

Fig. 7 describes the process flow, starting from the partial front-side processing of 525 μm thick wafers and continuing with the cavity etching and the implantation of a p^+ layer on the back-side and the p-spray on the front-side followed by a common thermal annealing. The processing finishes with the last metallization and passivation steps on the front-side [12]. The individual thinning steps are shown in Fig. 7. Thanks to the

optimized procedure, only small thickness fluctuations in the cavities were measured, up to a maximum value of 10 μm , even over the large surface of the quad sensors, see Fig. 8. A production carried out at MPG-HLL has been recently completed on 6" wafers. The handle wafers will be completely etched away after the Under Bump Bond Metal (UBM) processing at IZM Berlin.

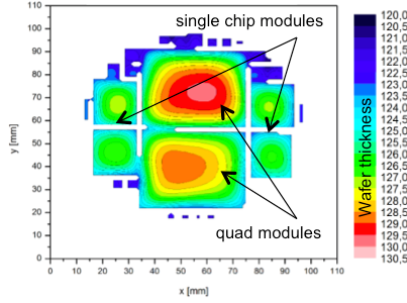


Figure 8: Thickness fluctuations within one wafer [12].

Before this step, the structures have been electrically characterized at wafer level by means of IV curves. Examples of the results are shown in Fig. 9 for the RD53 compatible sensors of 150 μm thickness. They show very low currents below 10 nA. The breakdown voltages are in the range of 150-250 V and well above the depletion voltage measured to be 15-20 V.

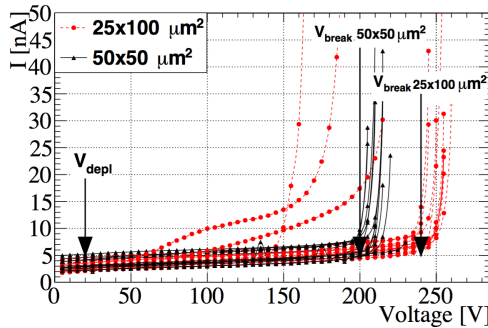


Figure 9: Test measurements on one MPG-HLL thin sensor wafer with small pixel cells of 50x50 and 25x100 μm^2 .

5. Summary and conclusions

Pixel modules were investigated for the upgrade of the ATLAS pixel system at HL-LHC. It has been shown that the main inefficiency regions coincide with the biasing structure of the pixel implants on the sensor front side. New punch-through structures with an external bias dot, common for four pixel cells and a new arrangement of the bias rail, have been studied for thicker sensors after an irradiation of $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ and compared to the standard design and to previous results at a fluence of $3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. It was found that the new structures yield a higher hit efficiency. Novel sensors were designed with

a combination of the two biasing structures and implemented in two thin sensor productions at CiS and MPG-HLL with 100-150 μm thin sensors, compatible to the new RD53 read-out chip. First measurements of sensors with a pixel cell of 50x50 and 25x100 μm^2 from the MPG-HLL production have been presented and show leakage currents below 10 nA and breakdown voltages well above the depletion voltages. Those sensors will be interconnected to the prototype chip of the RD53 Collaboration foreseen to be available in 2017. FE-I4 compatible sensors of the same productions will be in the meantime analyzed by means of test-beams to verify the radiation hardness up to fluences of $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$.

To allow for an investigation of the hit efficiency at high η at HL-LHC for the 50x50 μm^2 pixel cell, FE-I4 modules were tested in beam tests. The cluster properties were analyzed and a good hit efficiency extracted for the single pixels. Thinner sensors are found to be advantageous at high η for 50x50 μm^2 pixel cells given the lower cluster size and hence reduced occupancy expected in the innermost layer. Measurements of the samples after irradiation are planned to be performed with 100-150 μm thin sensors in a wider fluence range in the near future.

Acknowledgement

This work has been partially performed in the framework of the CERN RD50 Collaboration. The authors would like to thank A. Dierlamm for the irradiation at KIT.

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